WHAT IS CLAIMED IS:

1. A method for fabricating an MOS transistor, comprising:

forming a T-shaped gate electrode on a semiconductor substrate;

implementing a low-concentration ion implantation process using the gate electrode as an ion implantation mask to form a low-concentration impurity region in the semiconductor substrate on both sides of the gate electrode;

sequentially forming an L-shaped lower spacer, an L-shaped intermediate spacer, and an upper spacer on the low-concentration impurity region on both sides of the gate electrode;

removing the upper and intermediate spacers to expose the lower spacer; and

implementing a high-concentration ion implantation process into the semiconductor substrate where the lower spacer is exposed to form high- and mid- concentration impurity regions.

2. The method as claimed in claim 1, wherein forming the T-shaped gate electrode comprises:

forming a single layer conductive layer pattern on the semiconductor substrate; and

selectively etching the single layer conductive layer pattern such that an undercut region is formed.

3. The method as claimed in claim 2, wherein the gate electrode is polysilicon.

4. The method as claimed in claim 1, wherein forming the T-shaped gate electrode comprises:

forming lower and upper conductive layer patterns that are sequentially stacked on the semiconductor substrate; and

selectively etching the lower conductive layer pattern such that an undercut region is formed under an edge of the upper conductive layer pattern.

5. The method as claimed in claim 4, wherein the lower and upper conductive layer pattern are made of materials having an etch selectivity with respect to each other.

6. The method as claimed in claim 4, wherein the lower conductive layer pattern is made of silicon germanium or nitride titanium.

7. The method as claimed in claim 4, wherein the upper conductive layer pattern is made of polysilicon or tungsten.

8. The method as claimed in claim 4, wherein the selective etching of the lower conductive layer pattern employs an isotropic etch process.

9. The method as claimed in claim 1, further comprising conformally forming a surface insulating layer on an entire surface of the semiconductor substrate having the gate electrode.

10. The method as claimed in claim 1, wherein the lower spacer is formed of a material selected from the group consisting of nitride, oxynitride, and polysilicon.

11. The method as claimed in claim 1, wherein the intermediate spacer is made of a material having an etch selectivity with respect to the lower spacer.

12. The method as claimed in claim 11, wherein the intermediate spacer is formed from an oxide layer.

13. The method as claimed in claim 1, wherein the upper spacer is made of a material having an etch selectivity with respect to the intermediate spacer.

14. The method as claimed in claim 13, wherein the upper spacer is formed from a nitride layer.

15. The method as claimed in claim 1, wherein forming the upper spacer, the L-shaped intermediate spacer, and the L-shaped lower spacer comprises:

conformally forming lower, intermediate, and upper insulating layers that are sequentially stacked on an entire surface of the semiconductor substrate having the T-shaped gate electrode; and

successively etching the upper, intermediate, and lower insulating layers, wherein the upper insulating layer is etched using an anisotropic etch process.

16. The method as claimed in claim 1, further comprising:

forming a gate oxide layer on an entire surface of the semiconductor substrate before forming the gate electrode.

17. The method as claimed in claim 1, wherein the low-concentration ion implantation process is performed using an oblique ion implantation.

18. The method as claimed in claim 1, after implementing the high-concentration ion implantation process, further comprises:

forming a junction region silicide and a gate silicide at the high-concentration impurity region and on the upper conductive layer pattern, respectively.

19. The method as claimed in claim 18, wherein the junction region silicide and the gate silicide are formed of a material selected from the group consisting of cobalt silicide, nickel silicide, and tungsten silicide.

20. A MOS transistor comprising:

a T-shaped gate electrode disposed on a semiconductor substrate;

an L-shaped lower spacer covering a top surface of the semiconductor substrate at both sides of the gate electrode;

a low-concentration impurity region formed in the semiconductor substrate at both sides of the gate electrode;

a high-concentration impurity region formed in the semiconductor substrate next to the lower spacer; and

a mid-concentration impurity region disposed between the high- and low- concentration impurity regions.

21. The MOS transistor as claimed in claim 20, wherein the gate electrode comprises:

lower and upper conductive layer patterns that are sequentially stacked, wherein the upper conductive layer pattern is wider than the lower conductive layer pattern so as to have an

undercut region at a lower portion of the upper conductive layer pattern.

22. The MOS transistor as claimed in claim 21, wherein the L-shaped lower spacer further comprises a horizontal extension filling the undercut region.

23. The MOS transistor as claimed in claim 21, wherein the lower and upper conductive layer patterns are made of materials having an etch selectivity with respect to each other.

24. The MOS transistor as claimed in claim 21, wherein the lower conductive layer pattern is made of silicon germanium or nitride titanium.

25. The MOS transistor as claimed in claim 21, wherein the upper conductive layer pattern is made of polysilicon or tungsten.

26. The MOS transistor as claimed in claim 20, further comprising a surface insulating layer intervened between the gate electrode and the lower spacer.